ABSTRACT

The system and methods describe a computer system implementing an adjustable control

signal path whose length may be precisely adjusted to control timing of a control signal that

propagates along the path. One such adjustable signal path has two clusters of possible signal

5   paths. Each of the signal paths in each cluster has a length, and the overall length of the control

signal path may be adjusted by selectively implementing one signal path from each of the clusters

by electrically connecting that path into the electrical circuit by the selective installation of zero

ohm resistors. In this way, a system designer may design several possible signal path lengths on to

a motherboard or printed circuit card, and implement the path length which provides the most

10 precise signal timing adjustment.